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APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Seung-June KYOUNG a citizen of the Republic of Korea, residing at San 136-1, Ami-Ri, Bubal-Eub, Ichon-Shi, Kyoungki-Do 467-860, Korea have invented a new and useful APPARATUS FOR PROCESSING A BIT STREAM, of which the following is a specification.

APPARATUS FOR PROCESSING A BIT STREAM

Field of the Invention

The present invention relates generally to semiconductor devices; and, more particularly, to a bit stream processing apparatus for storing a bit stream in a circular buffer without separately storing a header and data of the bit stream.

Description of the Prior Art

Generally, an apparatus for processing a bit stream that is coded based on a frame sequentially stores the bit stream into a buffer and then processes the bit stream. Since the bit stream stored in the buffer is not aligned based on a byte or a word, and the number of bits required to process the bit stream is different for different cases, an aligner is needed for aligning the required bits.

FIG. 1 is a diagram showing a moving pictures expert group (MPEG) layer 3 audio frame format. As shown in FIG. 1, when the bit stream is coded based on a frame, a portion of the i-th frame data is stored in an unused portion of the (i-1)-th frame. Here, a pointer MB contained in a header H_i of the i-th frame F_i has a value identical to or smaller than zero and indicates a starting point of the i-th frame data stored in the (i-1)-th frame F_{i-1}.

For processing such a bit stream, additional hardware is needed for dividing the buffer into a header buffer and a data buffer and for decoding a header of the inputted bit stream to classify it as a header or as data. As a

result, the design of the bit stream processing unit is very complicated. Additionally, since different hardware is needed for different types of bit streams, a newly designed bit stream processing unit is required for processing each new type of bit stream.

Summary of the Invention

In accordance with an aspect of the invention, an apparatus is provided for processing a bit stream. The apparatus includes a circular buffer for storing a transmitted bit stream; a first register for storing data indicating a first read point of the bit stream stored in the circular buffer; and a first backup register for backing up the data stored in the first register. The apparatus also includes a second register for storing data indicating a number of bits to be read from the circular buffer; a third register for storing data indicative of the number of bits to be ignored from the read point; and a second backup register for backing up the data stored in the third register. In addition, the apparatus is provided with an adder for adding the data stored in the second register and the data stored in the third register; and a controller responsive to the adder to determine a number of bits to be shifted to read desired data from the circular buffer.

In accordance with another aspect of the invention, an apparatus is provided for reading data from a circular buffer storing data in a plurality of memory words. The apparatus includes a first storage device for storing data

indicative of a desired number of bits to be read; a second storage device for storing data indicative of a first bit to be read in a first memory word; and a shifter for receiving data stored in the first memory word and data stored in the second memory word located adjacent the first memory word in the circular buffer. The apparatus also includes a logic circuit in communication with the first and second storage devices for controlling the shifter to shift a number of bits specified by the data in the first and second storage devices to align the data in the shifter in a read position.

In accordance with another aspect of the invention, an apparatus is provided for reading data from a circular buffer storing data in a plurality of memory words which includes a first masking circuit and a second masking circuit. The first masking circuit receives data contained in at least two memory words of the circular buffer. The at least two memory words include data to be read. When a rightmost bit of the received data is not part of the data to be read, the first masking circuit outputs a subset of the received data which includes at least the data to be read but excludes at least the rightmost bit. The second masking circuit masks unwanted bits from the output of the first masking circuit.

In accordance with another aspect of the invention, a method is provided for reading data from a circular buffer storing data in a plurality of memory words. The method comprises the steps of: identifying at least one of the memory words containing data to be read; identifying a number of bits to

be read; identifying a first bit to be read; retrieving all data in the memory words of the circular buffer storing data to be read; inputting the retrieved data to a shifter; summing the number of bits to be read with a number of bits to be ignored adjacent the first bit to be read to develop a sum; subtracting the sum from a predetermined number to determine a shift amount; shifting the data in the shifter by the shift amount to remove unwanted bits adjacent a last bit to be read; masking unwanted bits adjacent the first bit to be read; and outputting the bits to be read.

Brief Description of the Drawings

The following description makes reference to the accompanying drawings, in which:

FIG. 1 is a diagram showing a moving pictures expert group (MPEG) layer 3 audio frame format;

FIG. 2 is a block diagram illustrating a bit stream processing unit constructed in accordance with the teachings of the present invention;

FIG. 3 is a diagram illustrating a sequence of transmitted bits in a circular buffer;

FIG. 4 is a block diagram for explaining an operation wherein 10 bits are read out in the first read mode of the bit stream processing unit shown in FIG. 2;

FIG. 4A is a schematic illustration showing a representative block of data received by the shifter 210;

FIG. 5 is a block diagram for explaining an operation wherein 13 bits are read out in the second read mode of the bit stream processing unit shown in FIG. 2;

FIG. 6 is a diagram illustrating each state of respective registers and backup registers in the bit stream processing unit when the operational mode is changed from the second read mode to the first read mode; and

FIG. 7 is a diagram illustrating an MPEG layer 3 audio frame format stored in the circular buffer.

Detailed Description of Preferred Examples

FIG. 2 is a block diagram illustrating a bit stream processing unit constructed in accordance with the teachings of the present invention. The bit stream processing unit of FIG. 2 includes a circular buffer 100, a head pointer register 110, a read pointer register 120, a read pointer backup register 130, a bit amount register 140, an adder 150, a shift amount controller 160, a shift amount register 170, a shift amount backup register 180, a remaining register 190, a remaining backup register 200, a shifter 210 and a masking circuit 220.

The circular buffer 100 stores a transmitted bit stream. The head pointer register 110 stores information indicating an address of the circular buffer 100 in which the transmitted bit stream is to be stored.

The read pointer register 120 indicates a memory word (X) of the bit stream stored in the circular buffer 100 wherein reading is to begin. The read pointer backup register 130 is used to backup the data stored in the read pointer register 120.

The bit amount register 140 stores the number of bits to be read from the circular buffer 100. The adder 150 adds the number of the bits stored in the bit amount register 140 and the number of bits to be ignored from the beginning of the memory word identified by the data in the read point register 120.

The shift amount controller 160 determines the amount of bits to be shifted in response to an output of the adder 150 to properly align the bits to be read. The shift amount register 170 stores data indicative of the number of bits to be ignored from the beginning of the memory word that is identified by the read point register 120. The shift amount backup register 180 is used to backup data stored in the shift amount register 170.

The remaining register 190 stores data from a memory word (X-1) of the bit stream in the circular buffer 100 adjacent the memory word (X) identified by the data in the read pointer register 120. The circular buffer 100 and the remaining backup register 200 are used to backup data stored in the remaining register 190.

The shifter 210 shifts data BUFF_OUT, which is stored in the memory word (X) of the circular buffer 100 indicated by the read pointer register 120

and data, which is stored in the remaining register 190 (i.e., memory word (X-1)), by a shift amount outputted from the shift amount controller 160 to thereby align the bits in a right direction. The masking circuit 220 masks unwanted bits to zero in response to a value stored in the bit amount register 140.

As shown in FIG. 2, since the illustrated bit stream processing unit includes respective backup registers 130, 180 and 200 for respective registers 120, 170 and 190, the bit stream can be read out a second time from a specific point when previous read data is stored in the backup registers.

First, it is assumed that one memory word (A[n]) of the circular buffer 100 includes 16 bits (e.g., A[n][15], A[n][14],..., A[n][0]). It is also assumed that the bit stream processing unit shown in FIG. 2 can align a maximum of 16 bits. FIG. 3 is a diagram illustrating a sequence of transmitted bits in the circular buffer 100.

The illustrated bit stream processing unit has two operational modes, namely, a first read mode and a second read mode. In the first read mode, a bit stream that is once read cannot be again read out. On the contrary, in the second read mode, a bit stream that is once read can be again read out.

In the first read mode, each value of the registers 120, 170 and 190 and each value of their respective backup registers 130, 180 and 200 are simultaneously updated.

In the second read mode, when each value of the registers 120, 170 and 190 is updated, each value of their respective backup registers 130, 180 and 200 is not updated.

FIG. 4 is a block diagram for explaining an operation wherein 10 bits are read out in the first read mode of the bit stream processing unit shown in FIG. 2. Here, it is assumed that the 10 bits to be read out are the 3 least significant bits (LSB) in memory word A[0] of the circular buffer 100 (e.g., A[0][2:0]) and the 7 most significant bits (MSB) in memory word A[1] (e.g., A[1][15:9]).

As shown in FIG. 4, since the read pointer register 120 points to an address of A[1], the remaining register 190 stores the 16 bits from memory word A[0]. Furthermore, the bit amount register 140 stores a value of 10 as the number of bits to be read, and the shift amount register 170 stores 13 bits as a consumed state because, in this example, we are not interested in the bits at address A[0][15:3].

Hereinafter, the operation of reading out 10 bits will be described in detail. The data stored in memory words A[0] and A[1] are input into the shifter 210, and the shift amount controller 160 outputs a value of 9 as a shift amount to the shifter 210. Here, the value of 9 is obtained by [32-(BIT_AMT+SH_AMT)], where BIT_AMT and SH_AMT denote values stored in the bit amount register 140 and the shift amount register 170, respectively. Thereafter, the shifter 210 shifts the 32 bits of A[0] and A[1] to

the right in response to the shift amount of 9 to thereby output 16 bits A[0][8:0]) and A[1][15:9]. Then, the masking circuit 220 masks 6 upper bits to zero and outputs {6'b0 (i.e., six upper bits zero), A[0][2:0], A[1][15:9]} as a final result.

The operation of the shift amount controller is explained in further detail in FIG. 4A. In particular, since we know the shifter 210 is to receive two memory words of data, namely, A[0] and A[1], and since we know each of those words is 16 bits long, the shifter 210 initially receiving 32 bits of data. We know from the shift amount register 170 that the data read is not to include the first 13 bits of data (labeled "A" in FIG. 4A) received at the shifter 210 (i.e., the read is to start at the 14th bit of memory word A[1]). We also know from the bit amount register 140 that the read is only to include 10 bits of data labeled "B" in FIG. 4A. Therefore, we know that the last 9 bits (32-13-10 = 9 bits labeled "C" in FIG. 4A received by the shifter are not to be included in the read. As a result, the shifter 210 shifts the received data 9 bits to the right to thereby place the ten bits of interest in the rightmost position of the shifter 210 (i.e., the "read position"). The masking circuit 220, which is adapted to only receive the rightmost word (i.e., the rightmost 16 bits) of the shifter 210, then zeros out the 6 upper bits of the word received from the shifter 210 based on the data stored in the bit amount register (i.e., 16 bits received from the shifter minus ten bits to be read equals 6 bits to be zeroed).

FIG. 5 is a block diagram for explaining an operation wherein 13 bits are read out in the second read mode of the bit stream processing unit shown in FIG. 2. The entire operation in FIG. 5 is the same as in FIG. 4, but in FIG. 5 (i.e., the second read mode) the backup registers 130, 180 and 200 respectively store the previous state for the registers 120, 170 and 190.

FIG. 6 is a diagram illustrating each state of the registers 120, 170 and 190 and the backup registers 130, 180 and 200 in the bit stream processing unit of FIG. 2 when the operational mode is changed from the second read mode shown in FIG. 5 to the first read mode. In particular, the data in backup registers 130, 180 and 200 is written to corresponding registers 120, 170 and 190.

Referring to FIG. 6, the values of the backup registers 130, 180 and 200 are restored to the respective registers 120, 170 and 190. Therefore, it is possible to repeat the previous data read when the operational mode is changed from the first mode to the second read mode.

FIG. 7 is a diagram illustrating an MPEG layer 3 audio frame format stored in the circular buffer. An operation of the bit stream processing unit of FIG. 2 will now be described with reference to FIG. 7.

Referring to FIG. 7, when data D_{i-1} of the (i-1)-th frame F_{i-1} is processed, the processed data need not be stored into a buffer so that the bit stream processing unit operates in the first read mode. Then, a header H_i of the i-th frame F_i is decoded in order to process data of the i-th frame F_i. At

this time, since data D_i stored in the (i-1)-th frame F_{i-1} will be required to complete the read operation, the bit stream processing unit changes its operational mode from the first mode to the second read mode. Then, by searching the header H_i of the i-th frame F_i and decoding a pointer MB, a location of the data D_i stored in the (i-1)-th frame F_{i-1} is identified. Thereafter, the apparatus retrieves the data from the identified location. Subsequently, the operational mode is changed to the first read mode, and the bit stream of the frame F_i stored in the (i-1)-th frame F_{i-1} is processed.

From the foregoing, persons of ordinary skill in the art will appreciate that a bit stream processing apparatus has been disclosed for storing a bit stream in one circular buffer without separately storing a header and a data of the bit stream.

Although preferred examples have been disclosed for illustrative purposes, those of ordinary skill in the art will appreciate that the scope of this patent is not limited to those examples. On the contrary, the scope of this patent extends to all structures and/or methods falling within the scope of the accompanying claims.